Palo Alto Compatible PAN-QSFP-40GBASE-LR4 Quick Spec:

Part Number:	PAN-QSFP-40GBASE-LR4 PAN-QSFP-40GBASE-LR4-EXT PAN-QSFP-40GBASE-LR4-IND
Form Factor:	QSFP
TX Wavelength:	1270nm-1330nm
Reach:	10km
Cable Type:	SMF
Rate Category:	40GBase
Interface Type:	CWDM-LR4
DDM:	Yes
Connector Type:	Dual-LC
Optical Power Budget:	6.7 dB
TX Power Min/Max:	-7 to +2.30 dBm
RX Power Min/Max:	-13.70 to +2.30 dBm

Palo Alto Compatible PAN-QSFP-40GBASE-LR4 Product Features

- Compliant with 40G Ethernet IEEE802.3ba and 40GBASE-LR4 Standard
- QSFP+ MSA compliant
- Compliant with QDR/DDR Infiniband data rates
- Up to 11.2Gbps data rate per wavelength
- 4 CWDM lanes MUX/DEMUX design
- Up to 10km transmission
- Operating case temperature:
  - Standard 0 to 70 °C
  - Extended -5 to +85 °C
  - Industrial -40 to +85 °C
- Maximum 3.5W operation power
- RoHS compliant

Palo Alto Compatible PAN-QSFP-40GBASE-LR4 Applications

- 40G BASE-LR4 Ethernet Links
- Infiniband QDR and DDR interconnects
- Client-side 40G Telecom connections
- 40Gb

Palo Alto Compatible PAN-QSFP-40GBASE-LR4 Overview

The PAN-QSFP-40GBASE-LR4 is a transceiver module designed for optical communication applications up to 10km. The design is compliant to 40GBASE-LR4 of the IEEE P802.3ba standard. The module converts 4 inputs channels of 10 Gbps electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 40Gbps optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 40 Gbps input into 4 CWDM channels signals, and converts them to 4 channel output electrical data. The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G694.2. It contains a duplex LC connector for the optical interface and a 148-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, singlemode fiber (SMF) has to be used. The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Palo Alto Compatible PAN-QSFP-40GBASE-LR4 Functional Diagram

This product converts the 4-channel 10 Gbps electrical input data into CWDM optical signals (light), by a driven 4-wavelength Distributed Feedback Laser (DFB) array. The light is combined by the MUX parts as a 40 Gbps data, propagating out of the transmitter module from the SMF. The receiver module accepts the 40 Gbps CWDM optical signals input, and de-multiplexes it into 4 individual 10Gbps channels with different wavelengths. Each wavelength is collected by a discrete avalanche photodiode (APD), and then outputted as electric data after amplified first by a TIA and then by a post amplifier. Figure 1 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

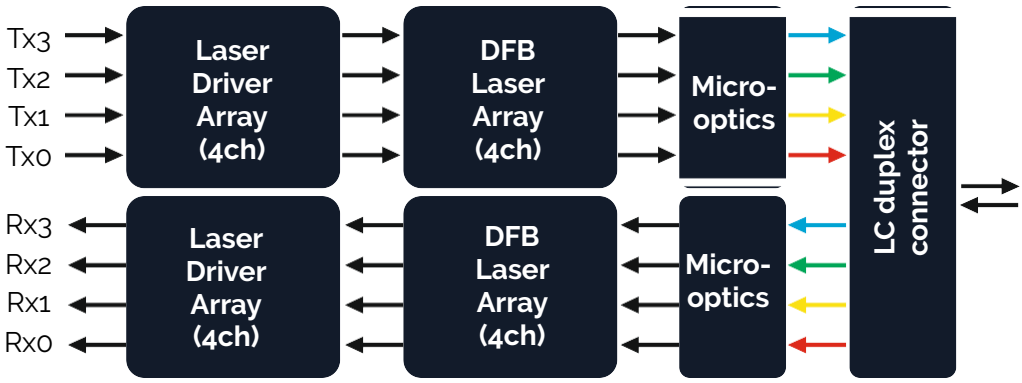


Figure 1. Functional diagram

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP+ memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground though a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. “Low” indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	*Tst*	-20	+85	°C
Relative Humidity (non-condensation)	RH		85	%
Operating Case Temp (Standard)	*Topc*	0	70	°C
Operating Case Temp (Industiral)	*Topc*	-40	85	°C
Operating Range		0.002	10	km

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vccl, VccTx, VccRx	-0.5		3.6	V
Data Rate, each Lane			10.3125	11.2	Gbps

Electrical Characteristics - Transmitter

Parameter	Symbol	Min	Typ	Max	Unit
Differential Input Impedance		85	100	115	Ohm
Differential Input Swing		150		1200	mV
TP1/TP1a Interface		Compliant to IEEE 802.3ba			

Electrical Characteristics - Receiver

Parameter	Symbol	Min	Typ	Max	Unit
Differential Output Impedance		90	100	110	Ohm
Differential Output Swing		370		950	mV
Receiver Electrical Mask		Compliant to IEEE 802.3ba			
Output Differential Return Loss		Compliant to IEEE 802.3ba			dB

Electrical Characteristics - Receiver

Parameter	Symbol	Min	Typ	Max	Unit
Wavelength Assignment	λ0	1264.5	1271	1277.5	nm
	λ1	1284.5	1291	1297.5	nm
	λ2	1304.5	1311	1317.5	nm
	λ3	1324.5	1331	1337.5	nm

Optical Characteristics - Transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Side-mode Suppression Ratio	*SMSR*	30			dB	
Total Average Launch Power	*PT*			8.3	dBm	
Average Launch Power (each Lane)		-7.0		2.3	dBm	
Optical Modulation Amplitude (each Lane)	*OMA*	-4		+3.5	dBm	
Difference in Launch Power between any two Lanes (OMA)				6.5	dB	
Launch Power in OMA minus Transmitter and		4.8			dBm	
Dispersion Penalty (TDP), each Lane						
TDP, each Lane	*TDP*			2.3	dB	
Extinction Ratio	*ER*	3.5			dB	
Relative Intensity Noise	*RIN*			-128	dB/Hz	12dB reflection
Transmitter Reflectance	*RT*			-12	dB	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Average Launch Power OF (each lane)	P_{off}			-30	dBm	

Note: Transmitter optical characteristics are measured with a single mode fiber.

Optical Characteristics - Receiver

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Damage Threshold	*THd*	3.3			dBm	1
Average Power at Receiver Input, each Lane		-13.7		2.3	dBm	
Receiver Reflectance	*RR*			-26	dB	
Receive Power (OMA) (each Lane)				3.5	dBm	
Receiver Power (OMA), each Lane				-9.9	dBm	
Receiver Power (OMA), each Lane	*Sr*			-11.5	dBm	
Difference in Receive Power between any two Lanes (OMA)				7.5	dB	
Receive Electrical 3 dB upper Cutoff Frequency, each Lane				12.3	GHz	
Vertical Eye Closure Penalty, each Lane			1.6		dB	
Stressed Eye Jitter, each Lane			0.3		UI	

Notes:

1. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

Digitial Diagnostics Function

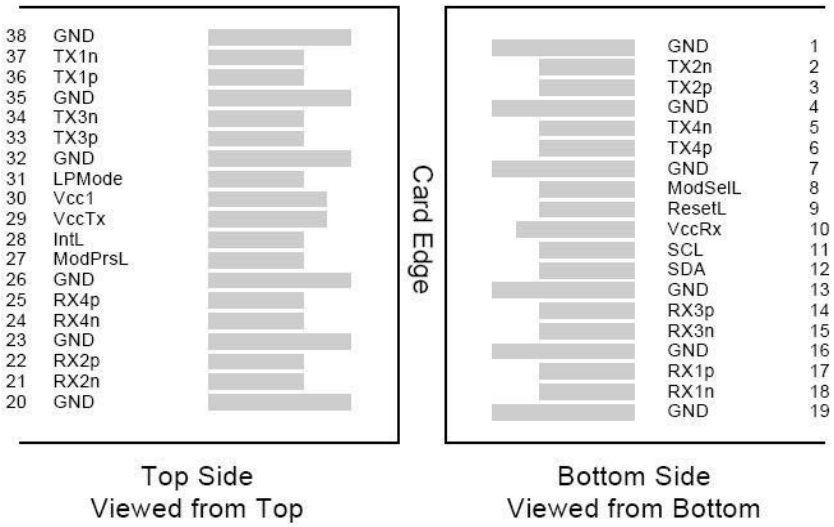
The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Temperature monitor absolute error	*DMITEMP*	-3		3	deg. C	Over operating temperature range
Supply voltage monitor absolute error	*DMIVCC*	-0.1		0.1	V	Over Full operating range
Channel RX power monitor absolute error	*DMIRX_CH*	-2		2	dB	1
Channel Bias current monitor	*DMIIbias_CH*	-10%		10%	mA	
Channel TX power monitor absolute error	*DMITX_CH*	-2		2	dB	1

Note 1: Due to measurement accuracy of different multi-mode fibers, there could be an additional ±1dB fluctuation, or ± 3dB total accuracy.

PIN Assignment and Function Definitions

PIN Assignment



PIN Definition

PIN	Signal Name	Description
1	GND	Ground (1)
2	Tx2n	CML-I Transmitter 2 Inverted Data Input
3	Tx2p	CML-I Transmitter 2 Non-Inverted Data Input
4	GND	Ground (1)
5	Tx4n	CML-I Transmitter 4 Inverted Data Input
6	Tx4p	CML-I Transmitter 4 Non-Inverted Data Input
7	GND	Ground (1)
8	ModSelL	LVTLL-I Module Select
9	ResetL	LVTLL-I Module Reset
10	VCCRx	+3.3V Power Supply Receiver (2)
11	SCL	LVCMOS-I/O 2-Wire Serial Interface Clock
12	SDA	LVCMOS-I/O 2-Wire Serial Interface Data
13	GND	Ground (1)
14	Rx3p	CML-O Receiver 3 Non-Inverted Data Output
15	Rx3n	CML-O Receiver 3 Inverted Data Output
16	GND	Ground (1)
17	Rx1p	CML-O Receiver 1 Non-Inverted Data Output
18	Rx1n	CML-O Receiver 1 Inverted Data Output
19	GND	Ground (1)
20	GND	Ground (1)
21	Rx2n	CML-O Receiver 2 Inverted Data Output
22	Rx2p	CML-O Receiver 2 Non-Inverted Data Output
23	GND	Ground (1)
24	Rx4n	CML-O Receiver 4 Inverted Data Output
25	Rx4p	CML-O Receiver 4 Non-Inverted Data Output
26	GND	Ground (1)
27	ModPrsL	Module Present
28	IntL	Interrupt
29	VCCTx	+3.3V Power Supply Transmitter (2)
30	VCC1	+3.3V Power Supply
31	LPMode	LVTLL-I Low Power Mode
32	GND	Ground (1)
33	Tx3p	CML-I Transmitter 3 Non-Inverted Data Input
34	Tx3n	CML-I Transmitter 3 Inverted Data Input
35	GND	Ground (1)
36	Tx1p	CML-I Transmitter 1 Non-Inverted Data Input
37	Tx1n	CML-I Transmitter 1 Inverted Data Input
38	GND	Ground (1)

Notes:

1. All Ground (GND) are common within the QSFP+ module and all module voltages are referenced to this potential unless noted otherwise. Connect these directly to the host board signal common ground plane.
2. V_{CC}Rx, Vcc1 and V_{CC}Tx are the receiving and transmission power suppliers and shall be applied concurrently. The connector pins are each rated for a maximum current of 500mA.

Licensing

The following U.S. patents are licensed by Finisar to FluxLight, Inc.:
U.S. Patent Nos: 7,184,668, 7,079,775, 6,957,021, 7,058,310, 6,952,531, 7,162,160, 7,050,720